REMARKS

Claim 5 has been amended to correct a typographical error as indicated by the

Examiner. The title has also been amended to add a missed space between two

independent words. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated

by Kim (US Pat. 6,078,543, "Kim" hereinafter). Claim 5 is amended and now claims 1-9

remain pending. Reconsideration and allowance of the application and presently pending

claims are respectfully requested.

Claim Objections

Claim 5 is objected to because of a typographical error. In response thereto,

Applicants have amended claim 5 to correct such error. As such, Applicants submit that

claim 5 is now in allowable form.

Claim Rejections 35 U.S.C. 102

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US

Pat. 6,078,543, "Kim" hereinafter).

In response to the rejections thereto, Applicants hereby otherwise traverse these

rejections. As such, Applicants submit that the method for independently refreshing a

memory capacitor, as set forth in claim 1, is novel and unobvious over Kim, or any of the

other cited references, taken alone or in combination, and thus should be allowed.

6

With respect to claim 1, as originally filed, recites in parts:

A method for independently refreshing a memory capacitor, for a system at least comprising a refresh controller coupled to an input terminal of a pre-decoded row address counter, ... said method comprising:

said pre-decoded row address counter counting a regular pre-decoded row address in response to said refresh control signal;

• • •

Applicants submit Kim at least failed to teach, suggest, or disclose, a system comprising a pre-decoded row address counter, and a method for refreshing a memory capacitor thereof, which comprises "the pre-decoded row address counter counting a regular pre-decoded row address in response to said refresh control signal" as required by claim 1.

Kim teaches a system comprising a "refresh counter 30" that "serves to sequentially generate an internal address during a refresh operation" (Column 1, lines 36 and 37), and both the internal address and an external address are inputted to an "X-address predecoder 50" that "outputs the upper coding signal and the lower coding signal by decoding the internal address from the refresh counter 30" (Column 2, lines 62-64). Therefore, in accordance with the teaching of FIG. 1, Kim teaches the X-address predecoder 50 receives internal addresses from the refresh counter 30, and the decoding process is performed after obtaining the internal address from the refresh counter 30. Thus, the decoding process is performed by the X-address predecoder 50 after receiving the internal address from the refresh counter 30.

Accordingly, a "pre-decoded row address counter, that should be interpreted as for

counting pre-decoded row addresses" as claimed in claim 1, is neither taught, disclosed, nor suggested by Kim, or any of the other cited references, taken alone or in combination.

Further, addressing the step of "the pre-decoded row address counter counting a regular pre-decoded row address in response to said refresh control signal", the Examiner contended that it has been taught by Kim in column 1, lines 37-48 and column 2, lines 58-64. However, on the contrary, Kim only teaches "the refresh counter 30 serves to sequentially generate an internal address during a refresh operation", and "the X-address predecoder 50 outputs the upper coding signal and the lower signal by decoding the internal address from the refresh counter 30," but does not teach "counting a regular pre-decoded row address". There is no teaching that such a refresh counter 30 is used for dealing with pre-decoded addresses in Kim, and, on the contrary, in Kim, the internal address is decoded only after the being received by the X-address predecoder 50.

Therefore, for at least the foregoing reasons, Applicants submit that Kim fails to teach each and every elements of the claimed invention, as set forth in claim 3. As such, claim 1 and its dependent claim 2 are submitted to be novel and unobvious over Kim, or any of the other cited references, taken alone or in combination, and thus should be allowed.

Similarly, claim 3, as originally filed, recites in parts:

An apparatus for refreshing a memory capacitor, comprising:

a pre-decoded row address counter, said pre-decoded row address counter comprising a plurality of pre-decoded row address lines, said pre-decoded row address counter being couple to said refresh controller and receiving said refresh control signal to count, said pre-decoded row address counter outputting a regular pre-decoded row address in response to said refresh

control signal via said pre-decoded row address lines;

...

For similar reason as discussed above, Applicants submit that Kim fails to teach an apparatus comprising: "a pre-decoded row address counter ... comprising a plurality of pre-decoded row address lines, ..., said pre-decoded row address counter counting a regular pre-decoded row address ...". Applicants submit that what is taught by Kim shows that only by the X-address predecoder 50, which is arranged after the refresh counter 30, the internal addresses could be decoded, and none of the addresses have been taught to be pre-decoded before or during the pre-decoded row address counter processing. As such, Applicants submit that Kim fails to teach each and every elements of the claimed invention, as set forth in claim 3. As such, claim 3 is submitted to be novel and unobvious over Kim, or any of the other cited references, taken alone or in combination, and thus should be allowed.

Claims 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim, as supported by the US patent to Haga (6,104,657).

Applicants submit that claims 4-9 depend on allowable claim 3, and thus should also be allowable.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-9 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: Oct. 5,2006

Respectfully submitted,

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office 7th Floor-1, No. 100 Roosevelt Road, Section 2 Taipei, 100 Taiwan

Tel: 011-886-2-2369-2800 Fax: 011-886-2-2369-7233

Email: <u>belinda@jcipgroup.com.tw</u> <u>Usa@jcipgroup.com.tw</u>